Control and Experiment of AC/AC Sparse Modular Multilevel Converter

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***Abstract*—The sparse modular multilevel converter (MMC) is a new type of high-voltage ac/ac MMC topology suitable for high-power applications. It is based on an alternative configuration of half/full-bridge submodules, and voltage unfolder stages on each side of the converter. This topology has fewer components compared to conventional approaches and as an additional benefit, more than half of the switches operate under the soft switching condition. A comprehensive control strategy is proposed to ensure capacitor voltage balancing while exploiting the full power capability of the converter. A modified unfolder is also suggested to eliminate the inherent zero-crossing circulating current. The effectiveness of the proposed control strategy is confirmed by simulation and experimental results.**

***Index Terms*—Sparse modular multilevel converter, MMC, capacitor voltage balancing, third harmonic injection, soft switching.**

I. Introduction

WITH THE ever increasing advancement in semiconductor devices, high power voltage source converters (VSCs) have been attracting more attention in many industrial applications such as renewable energy resource interfaces, flexible AC transmission system (FACTS) devices and HVDC lines [1]–[3]. In many of these applications, two AC networks with different frequencies are connected, or variable frequency capability is desired. Fractional Frequency Transmission System (FFTS) is an example that uses low frequency to reduce the line reactance, and to increase its capacity. FFTS has been used in European railway electrification systems for almost a century [4], [5]. Recently, AC/AC converters were proposed to reduce the weight and losses in traction propulsion systems [6]–[8]. Other examples are high voltage machine drives [9]–[11]. A back-to-back (B2B) 2-level VSC is a well-known topology that uses a DC-link to connect two AC sources [12]. Several topologies are proposed to reduce its component count, yet they face limitations in the modes of operation and may require complex control systems [13]–[15]. For higher voltage levels, B2B multilevel converters are normally used as they can provide high voltage output with extremely low distortion and lower dv/dt, while the semiconductor devices only have to tolerate a portion of the DC voltage [16]–[18]. The complexity of the capacitor voltage balancing in diode-clamped converter (DCC) [19], [20] is solved in the B2B version [21], yet similar to flying capacitor converter (FCC) and cascaded H-bridge converters (HBC), it suffers from high number of components.

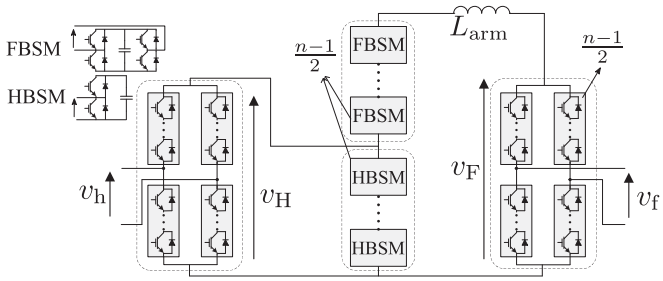

Fig. 1. Schematic diagram of a single-phase n-level SMMC.

Modular multilevel converter (MMC) is proposed in 2003 to overcome such limitations by utilizing low voltage switches and offering low harmonic distortion [22]. Currently, MMC-based HVDC systems are offered for power transmission up to GW ranges [23]. Modular multilevel matrix converter is first introduced in 2001 [24] and then further got developed for motor drive applications [25]. High number of hard-switched semiconductors and undesired circulating currents are the drawbacks of MMC and modular multilevel matrix converter which are considerably improved in Sparse Modular Multilevel Converter (SMMC) [26]. In this paper, a control strategy based on third-harmonic injection is proposed for SMMC to guarantee the capacitor voltage balancing in different operational conditions. In addition, a modified unfolder is suggested to eliminate the inherent zero-crossing circulating current. The rest of the paper is organized as follows.

First, a brief description on eliminating zero-crossing circulating current is discussed in Section II. Section III presents the theoretical analysis of capacitor voltage balancing. This is followed by implementing a control strategy based on the theoretical findings in Section IV. The functionality of the proposed voltage balancing control system, is confirmed by both simulation and experiment in Section V and VI, respectively. Finally, Section VII presents the conclusions.

II. Modified Sparse Modular Multilevel Converter

Fig. 1 shows the schematic diagram of a single phase Sparse Modular Multilevel Converter (SMMC) [26]. The SMMC consists of two low frequency unfolders on the sides and one leg

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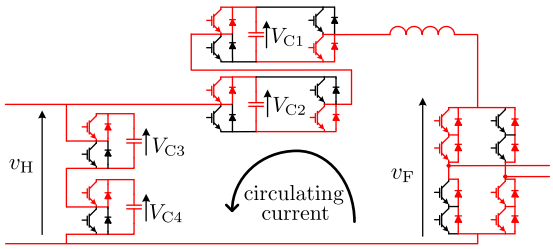

Fig. 2. Zero-crossing circulating current in a 5-level SMMC.

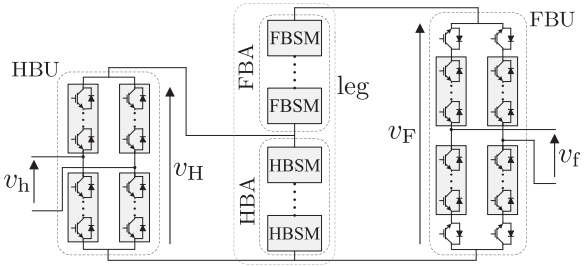

Fig. 3. Schematic diagram of a modified single-phase SMMC.

containing a number of cascaded full-bridge (FBSM) and half-bridge submodules (HBSM). By inserting proper number of SMs in the upper and lower arms, the desired voltage on both sides of the converter can be achieved. Unlike MMC, there is no circulating current between different legs (phases) of SMMC, as they are isolated from each other by a 3-phase transformer. However, it is inherently possible for current to circulate inside one phase of the SMMC. This current is not continuous and may only flow when v_F crosses zero, and so it is called zero-crossing circulating current. For example, in Fig. 2, if $V_{C3} + V_{C4}$ is slightly smaller than $V_{C1} + V_{C2}$, it causes v_F to become a small negative value (when $v_F = 0$ is required). In addition, due to switching transients, the SM insertion/bypassing may not occur simultaneously. This leads to one extra level decrease/increase in v_F for a short period of time. An extra level decrease in v_F (when $v_F = 0$ is required), could make v_F negative. This negative voltage turns on the unfolder's anti-parallel diodes and current circulates through the leg. The arm inductor is installed to limit this current.

Two major factors in determining the cost of arm inductor are its inductance [26] and its nominal current. This inductor is on the path of the entire transferred power, thus it must be able to continuously withstand the total current without saturation which makes it a big passive component almost as comparable to the AC-filter inductor. Adding one reversed IGBT in each arm of the FB-side Unfolder (FBU) could block the possible small negative v_F as shown in Fig. 3 and obviates the necessity of the arm inductor. The HB-side unfolder (HBU) remains intact. It should be noticed that the maximum voltage-drop across the reversed IGBT occurs, when half-bridge arm (HBA) and full-bridge arm (FBA) capacitors are in their lowest and highest acceptable voltages, respectively. Therefore, this IGBT must withstand the predefined capacitor voltage ripple, ΔV_{ripp} multiplied by the number of HBSMs (or FBSMs) which equals to $(n-1)/2 \times \Delta V_{ripp}$. This implies that in case

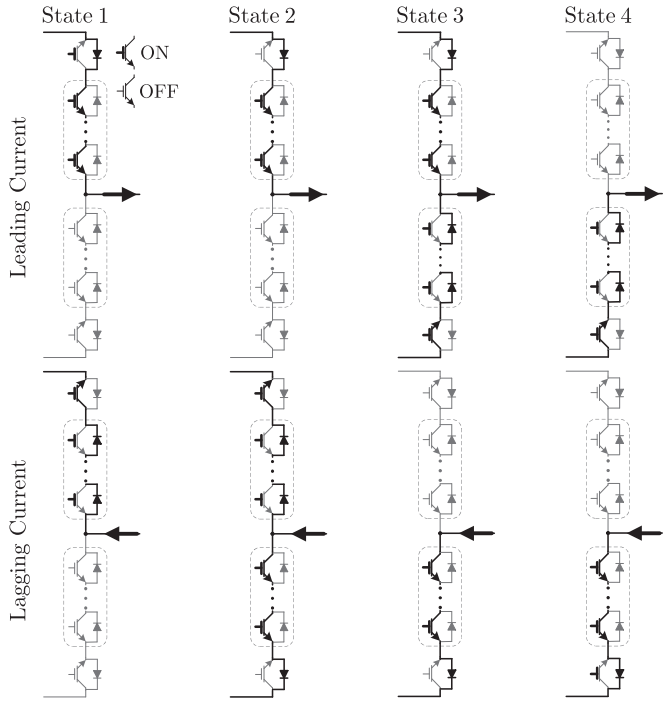

Fig. 4. Description of zero-crossing transition in FBU.

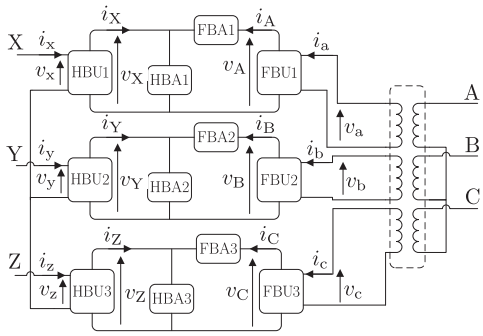

Fig. 5. Schematic diagram of a 3-phase SMMC.

of high number of levels, more than one reversed IGBT might be required.

The additional IGBT is part of the unfolder arm which is a string of series-connected semiconductor devices. This requires both transient and steady-state voltage sharing among the devices. The unfolders operate in zero-voltage switching (ZVS) mode, thus transient voltage sharing is always satisfied [26]. In the off-state, steady-state voltage sharing is achieved by installing high-value parallel resistors. The additional IGBT must be equipped with the same resistor. Fig. 4 demonstrates FBU's principle of operation at voltage zero-crossing transition for both leading and lagging currents. It can be seen that at any stage of transition, there is at least one reversed IGBT blocking the zero-crossing circulating current. The 3-phase SMMC is constructed using a 3-phase transformer as shown in Fig. 5.

III. Capacitor Voltage Balancing

Fig. 6 shows the simplified schematic diagram of a single-phase SMMC. The voltages and currents on the FB- and

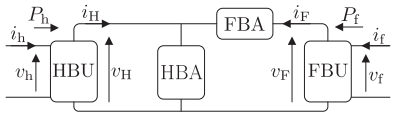

Fig. 6. Simplified schematic diagram of a single-phase SMMC.

HB-sides of the converter can be represented as:

$$\begin{cases} v_{\rm f} = V_{\rm mf}\sin(\omega_{\rm f}t),\ v_{\rm F} = \lambda_{\rm f}.v_{\rm f},\ \lambda_{\rm f} = \text{sign}(v_{\rm f}) \\ i_{\rm f} = I_{\rm mf}\sin(\omega_{\rm f}t - \varphi_{\rm f}),\ i_{\rm F} = \lambda_{\rm f}.i_{\rm f} \end{cases} \tag{1}$$

$$\begin{cases} v_{\rm h} = V_{\rm mh}\sin(\omega_{\rm h}t + \theta_{\rm h}),\ v_{\rm H} = \lambda_{\rm h}.v_{\rm h},\ \lambda_{\rm h} = \text{sign}(v_{\rm h}) \\ i_{\rm h} = I_{\rm mh}\sin(\omega_{\rm h}t + \theta_{\rm h} - \varphi_{\rm h}),\ i_{\rm H} = \lambda_{\rm h}.i_{\rm h} \end{cases} \tag{2}$$

According to Fig. 6, the instantaneous power going through FBA and HBA are calculated as:

$$p_{\rm HB}(t) = (i_{\rm F} + i_{\rm H}) \times v_{\rm H},\ p_{\rm FB}(t) = i_{\rm F} \times (v_{\rm F} - v_{\rm H}). \tag{3}$$

In the steady-state condition, the stored energy of FBA and HBA must be constant, so the capacitor voltages remain unchanged. This leads to the following equations:

$$\int_T p_{\rm HB}(t).dt = 0,\ \int_T p_{\rm FB}(t).dt = 0. \tag{4}$$

Eq. (4) is rewritten as following criteria:

$$\int_T \left(p_{\rm FB}(t) + p_{\rm HB}(t)\right).dt = 0\ ,\ \int_T p_{\rm FB}(t).dt = 0. \tag{5}$$

The first criterion leads to the real power balance between the AC-sides as presented below:

$$\begin{aligned} 0 &= \int_T \left(p_{\rm FB}(t) + p_{\rm HB}(t)\right).dt \\ &= \int_T (i_{\rm F} \times v_{\rm F} + i_{\rm H} \times v_{\rm H}).dt \\ &= \frac{1}{2}V_{\rm mf}I_{\rm mf}\cos(\varphi_{\rm f}) + \frac{1}{2}V_{\rm mh}I_{\rm mh}\cos(\varphi_{\rm f}) \\ &\Rightarrow P_{\rm f} + P_{\rm h} = 0. \end{aligned} \tag{6}$$

The second criterion is studied as:

$$\begin{aligned} 0 = \int_T p_{\rm FB}(t).dt &= \int_T \{i_{\rm F} \times (v_{\rm F} - v_{\rm H})\}.dt \\ \Rightarrow \frac{1}{2}V_{\rm mf}I_{\rm mf}\cos(\varphi_{\rm f}) &= \int_T (i_{\rm F} \times v_{\rm H}).dt \\ = V_{\rm mh}I_{\rm mf}\int_T \{\lambda_f \sin(\omega_f t - \varphi_{\rm f})\,|\sin(\omega_{\rm h}t + \theta_{\rm h})|\}.dt. \end{aligned} \tag{7}$$

This can be rewritten as:

$$\begin{aligned} \frac{V_{\rm mf}}{V_{\rm mh}} &= \int_T \frac{2\lambda_{\rm f}\sin(\omega_{\rm f}t - \varphi_{\rm f})\,|\sin(\omega_{\rm h}t + \theta_{\rm h})|}{\cos(\varphi_{\rm f})}.dt \\ &= \int_T g(t).dt - \int_T h(t).dt, \\ g(t) &= 2\,|\sin(\omega_{\rm f}t)\sin(\omega_{\rm h}t + \theta_{\rm h})|\,, \\ h(t) &= 2\lambda_{\rm f}\cos(\omega_{\rm f}t)\tan(\varphi_{\rm f})\,|\sin(\omega_{\rm h}t + \theta_{\rm h})|\,. \end{aligned} \tag{8}$$

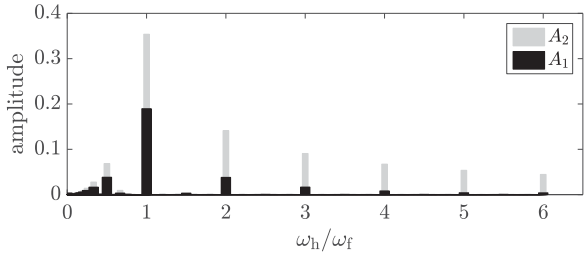

Fig. 7. The value of A_1 and A_2 based on $\omega_{\rm h}/\omega_{\rm f}$.

There is no analytical solution for Eq. (8). However, its numerical solution can be approximated as:

$$G = \int_T g(t) \approx 0.81 + A_1\cos(B.\theta_{\rm h}), \tag{9}$$

$$H = \int_T h(t) \approx A_2\tan(\varphi_{\rm f})\sin(B.\theta_{\rm h}). \tag{10}$$

where A_1 and A_2 are positive real numbers which only depend on the frequency ratio ($\omega_{\rm h}/\omega_{\rm f}$) as shown in Fig. 7. By substituting Eqs. (9) and (10) in Eq. (8):

$$\begin{aligned} &\frac{V_{\rm mf}}{V_{\rm mh}} = .81 + A_1\cos(B\theta_{\rm h}) - A_2\tan(\varphi_{\rm f})\sin(B\theta_{\rm h}) \\ &\Rightarrow (0.81 - M) \le \frac{V_{\rm mf}}{V_{\rm mh}} \le (0.81 + M) \end{aligned} \tag{11}$$

where, $M = \sqrt{A_1^2 + A_2^2\tan(\varphi_{\rm f})^2}$. Finally, the voltage balancing criteria can be summarized as:

$$P_{\rm f} + P_{\rm h} = 0,\ (0.81 - M) \le \frac{V_{\rm mf}}{V_{\rm mh}} \le (0.81 + M). \tag{12}$$

A. The impact of frequency ratio

Assume the AC-side frequencies are not an integer multiple of each other ($\omega_{\rm h}/\omega_{\rm f} \neq m$ or $1/m$ where m is an integer number). In this case, as it is shown in Fig. 7, A_1 and A_2 are constant and almost equal to 0. For instance, if the converter operates between two grids with the frequencies of 50 Hz and 60 Hz, $A_1 = 0.0001$ and $A_2 = 0.0028$. Assuming that $v_{\rm f}$ side is not purely inductive, by substituting A_1 and A_2 in Eq. (11):

$$M \approx 0 \Rightarrow \frac{V_{\rm mf}}{V_{\rm mh}} \approx 0.81. \tag{13}$$

Thus, the AC-side voltage ratio equals 0.81 regardless of the frequency ratio. According to Eq. (11), even if the frequency ratio is a small integer number, the voltage ratio would still be constant, but it could be affected by AC-sides power factor and phase-angle. In other words, if voltage balancing is achieved, the converter's gain is always a fixed value. In the next section, third harmonic injection is proposed to regulate the converter's gain, regardless of the frequency ratio.

B. Voltage Ratio Regulation

For many practical applications, voltage ratio control is vital. For example, in grid-connected application, voltage gain can be used to adjust the reactive power exchange with the AC

networks. The AC-side voltages can be controlled by injecting harmonics, such that the ratio between the average rectified AC voltage and its fundamental component is adjusted. In this process, the unfolders are preferred to retain the soft switched operation. In general, both sides of the converter can contribute to the voltage ratio control by admitting an infinite series of harmonics. However, the added harmonics should be chosen such that they are cancelled out in line-line voltages. In other words, only odd multiples of three harmonics $(3, 9, 15, 21, \ldots, \infty)$ can be used. As an example, the voltage control is performed using only third harmonic addition to transformer-side of the converter (see Fig. 5). Based on this strategy, the AC-side voltages in a 3-phase SMMC shown in Fig. 5 can be represented as:

$$\begin{cases} v_{\rm a} = V_{\rm mf}\sin(\omega_{\rm f}t) + V_3\sin(3\omega_{\rm f}t+\beta) \\ v_{\rm b} = V_{\rm mf}\sin(\omega_{\rm f}t - 2\pi/3) + V_3\sin(3\omega_{\rm f}t+\beta) \\ v_{\rm c} = V_{\rm mf}\sin(\omega_{\rm f}t - 4\pi/3) + V_3\sin(3\omega_{\rm f}t+\beta) \\ v_{\rm U} = \lambda_{\rm u}v_{\rm u},\ \lambda_{\rm u} = \text{sign}(v_{\rm u}),\ {\rm u} = {\rm a,b,c} \end{cases} \tag{14}$$

$$\begin{cases} v_{\rm x} = V_{\rm mh}\sin(\omega_{\rm h}t + \theta_{\rm h}) \\ v_{\rm y} = V_{\rm mh}\sin(\omega_{\rm h}t + \theta_{\rm h} - 2\pi/3) \\ v_{\rm z} = V_{\rm mh}\sin(\omega_{\rm h}t + \theta_{\rm h} - 4\pi/3) \\ v_{\rm U} = \lambda_{\rm u}v_{\rm u},\ \lambda_{\rm u} = \text{sign}(v_{\rm u}),\ {\rm u} = {\rm x,y,z} \end{cases} \tag{15}$$

Now, it is desired to develop voltage balancing equations for one phase of the SMMC (e.g. the phase between A and X). According to Fig. 5, the instantaneous power going through FBA1 and HBA1 are:

$$p_{\rm HB1}(t) = (i_{\rm A} + i_{\rm X}) \times v_{\rm X},\ p_{\rm FB1}(t) = i_{\rm A} \times (v_{\rm A} - v_{\rm X}). \tag{16}$$

Similar to the previous section, the capacitor voltage balancing criteria can be defined as:

$$\int_T \left(p_{\rm FB1}(t) + p_{\rm HB1}(t)\right).dt = 0,\ \int_T p_{\rm FB1}(t).dt = 0. \tag{17}$$

The neutral terminal of the transformer is not grounded, thus the added third harmonic voltage does not create current and thus cannot contribute to the power flow. As a result, similar to previous section, the first criterion of voltage balancing leads to the real power balance between the AC-sides. The second criterion of voltage balancing eqs. leads to:

$${\rm VR} = \frac{V_{\rm mf}}{V_{\rm mh}} = \int_T \frac{2\lambda_{\rm a}\sin(\omega_{\rm f}t - \varphi_{\rm f})\,|\sin(\omega_{\rm h}t+\theta_{\rm h})|}{\cos(\varphi_{\rm f})}.dt. \tag{18}$$

The impact of phase angle $\theta_{\rm h}$ and frequency ratio are studied before. Thus, for simplicity, in this section, it is assumed that $\theta_{\rm h} = 0$ and also the frequency ratio is not a small integer number. The ratio of AC-side voltages can be calculated as:

$$\begin{cases} {\rm VR} = \dfrac{V_{\rm mf}}{V_{\rm mh}} = \displaystyle\int_T g(t) - \int_T h(t), \\ g(t) = 2\lambda_{\rm a}\sin(\omega_{\rm f}t)\,|\sin(\omega_{\rm h}t)|\,, \\ h(t) = 2s(t)\tan(\varphi_{\rm f}), \\ s(t) = 2\lambda_{\rm a}\cos(\omega_{\rm f}t)\,|\sin(\omega_{\rm h}t)|\,, \end{cases} \tag{19}$$

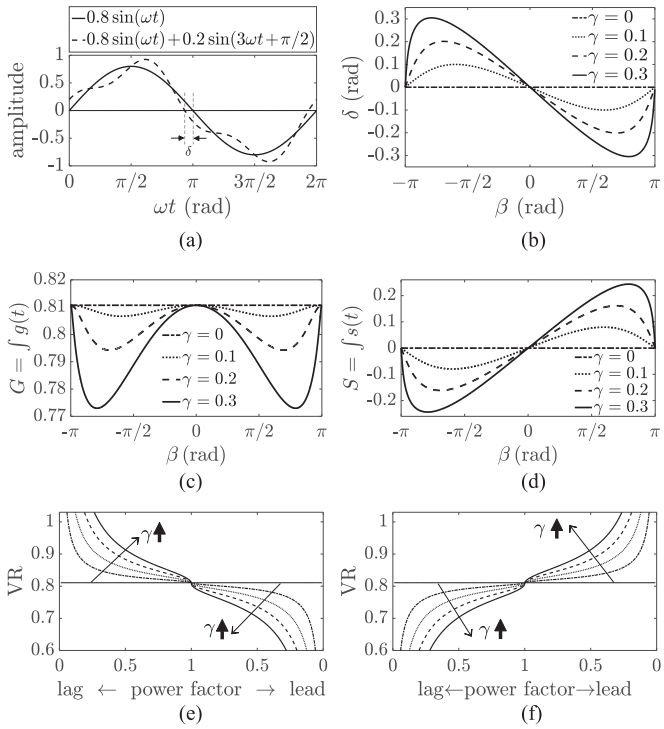

Fig. 8. (a) Adding third harmonic voltage shifts the zero-crossing point (b) The value of δ regarding to different β (c) The value of G due to variation of third harmonic injection (d) The value of S due to variation of third harmonic injection (e) The voltage ratio due to variation of γ ($\beta = -0.8\ \pi$) (f) The voltage ratio due to variation of γ ($\beta = 0.8\ \pi$).

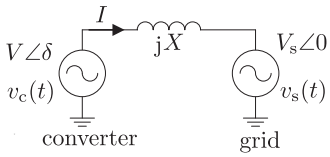

Fig. 9. Simplified single-line diagram of converter-grid circuit.

where, $\lambda_{\rm a}$ is calculated as:

$$\begin{aligned} \lambda_{\rm a} &= \text{sign}(V_{\rm mf}\sin(\omega_{\rm f}t) + V_3\sin(3\omega_{\rm f}t+\beta)) \\ &= \text{sign}(\sin(\omega_{\rm f}t) + \gamma\sin(3\omega_{\rm f}t+\beta)), \\ \gamma &= \frac{V_3}{V_{\rm mf}},\ -\pi \le \beta \le \pi. \end{aligned} \tag{20}$$

Adding third harmonic voltage would appear as a phase-angle shift in $\lambda_{\rm a}$, such that the zero-crossing point of the target AC voltage is shifted by δ (rad) without affecting the fundamental component as shown in Fig. 8a. Different values of δ could be achieved by adjusting γ and β in Eq. (20) as shown in Fig. 8b. The behavior of $\int g(t)$ and $\int s(t)$ regarding to different amount of third harmonic injection (γ, β) are illustrated in Figs. 8c and 8d respectively. By considering the impact of power factor in Eq. (19), the voltage ratio of the converter is sketched for $\beta = -0.8\ \pi$ and $\beta = 0.8\ \pi$, as shown in Figs. 8e and 8f respectively.

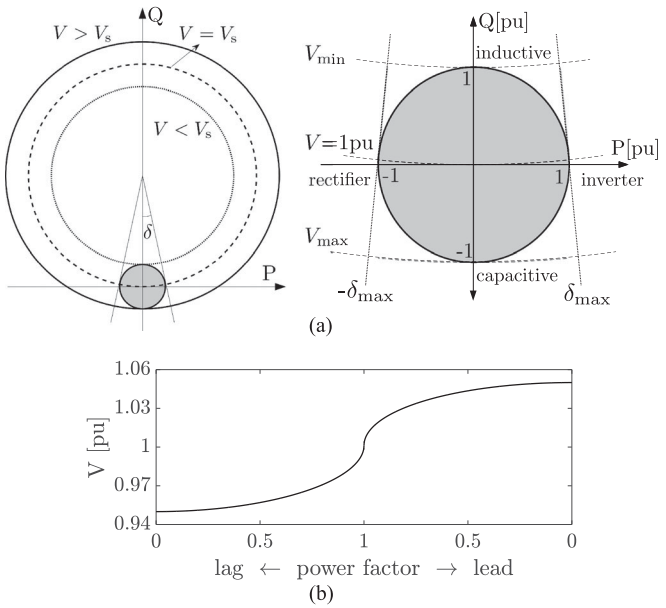

Fig. 10. (a) The power capability chart of SMMC (b) required SMMC's output voltage in different power factor (inverter mode).

C. Impact of SMMC's gain on its Power Capability

Fig. 9 shows the simplified single-line diagram of converter-grid circuit. The injected active and reactive powers to the grid are calculated as:

$$P = \frac{VV_{\rm s}}{X}\sin\delta,\ Q = \frac{V_{\rm s}^2 - VV_{\rm s}\cos\delta}{X} \tag{21}$$

where $V\angle\delta$ and $V_{\rm s}\angle 0$ are the voltage phasors of converter's AC-side and grid, respectively and X is the filter reactance. To study the impact of converter's gain, it is assumed that $V_{\rm s} = 1$ pu. From Eq. (21), the PQ diagram of the SMMC is both sketched regardless of the converter's limitation and also considering the maximum tolerable IGBT's current as magnified in Fig. 10a. The typical value of 0.05 pu is assumed for the filter reactance. Considering $Q = \pm$ 1 pu in Eq. (21), the range of converter's output voltage is equal to $V_{\rm min} = 0.95$ and $V_{\rm max} = 1.05$ as shown in Fig. 10b for inverter mode. From the previous section, the required injected third harmonic voltage for this SMMC is in the range of $-0.10 \leqslant \gamma \leqslant 0.10$.

IV. Control Strategy

The proposed converter could be controlled in either abc-frame where PR controller is used [27], [28] or in dq-frame as shown in Fig. 11. To control the AC-side currents in dq-frames, a synchronization mechanism is achieved through a Phase-Locked Loop (PLL) on each side of the converter with capability of input DC-error rejection [29]. Two reference generators are utilized to provide the reference AC currents for the next control stage. $P_{\rm fref}$ in Grid F, determines the amount and direction of transferred real power, while the reactive powers, $Q_{\rm fref}$ and $Q_{\rm href}$ are regulated to arbitrary values within the rating of converter. On each side of the converter, a standard current controller is used as depicted in Fig. 12, which provides the expected active and reactive power exchange with the grid.

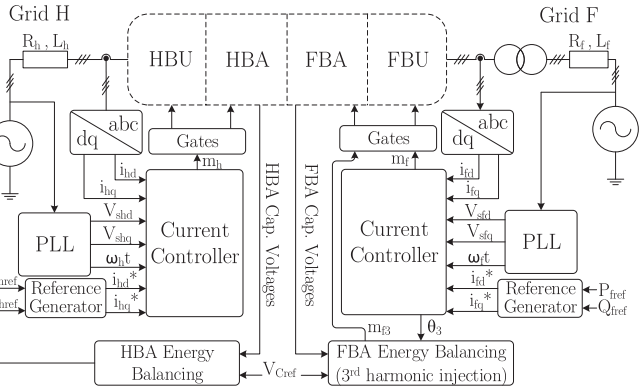

Fig. 11. The schematic diagram of control strategy.

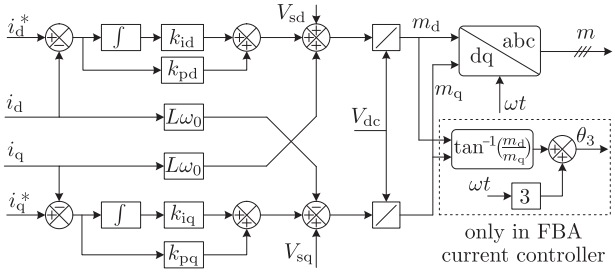

Fig. 12. The schematic diagram of the current controller.

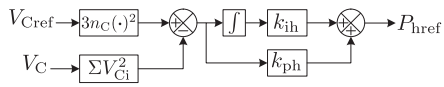

Fig. 13. The schematic diagram of HBA Energy Balancing unit.

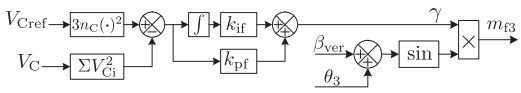

Fig. 14. The schematic diagram of FBA Energy Balancing unit.

If the capacitor voltages have some oscillations, harmonics can be rejected from the AC-side currents and voltages if a modified PWM is used [30].

To regulate the total energy stored in the capacitors, a slow outer control loop is employed on each side of the converter. To do so, the capacitor voltage reference ($V_{\rm Cref}$) and its measured value are squared and multiplied by the total number of SMs in the arm, which provides the desired and measured energy stored in the arm. By adjusting the total energy stored in the arm capacitors, the balance between the arm power and the AC-side active power is maintained. For the HB-side, the internal control variable of $P_{\rm href}$ is provided according to the total energy stored in the HBAs as illustrated in Fig. 13. $n_{\rm C}$ is the total number of capacitors in each arm which is equal to $(n-1)/2$ in an n-level SMMC. For the FB-side, as mentioned in the previous section, the power flow could be controlled by injecting third harmonic voltage. Fig. 14 illustrates the process of providing γ which then is used to generate the third harmonic component. $\beta_{\rm ver}$ ($\approx 0.8\ \pi$ or $-\ 0.8\ \pi$) is the phase angle that generates the highest/lowest voltage ratio. It is also necessary to evenly distribute the arm energy between the capacitors by selecting

TABLE I
SIMULATION PARAMETERS

Parameter		Rating
Power rating	$S_{\mathrm{conv.}}$	4 MVA
Grid H & F frequencies	f_{h}, f_{f}	60 Hz, 50 Hz
Grid H & F voltages (line-line rms)	V_{Sh}, V_{Sf}	9 kV, 7.3 kV
SM capacitor	C_{SM}	4 mF
Mean cell capacitor voltage	E	2000 V
Filter + Grid inductance	L_{f}, L_{h}	5 mH
Filter + Grid resistance	R_{f}, R_{h}	10 mΩ

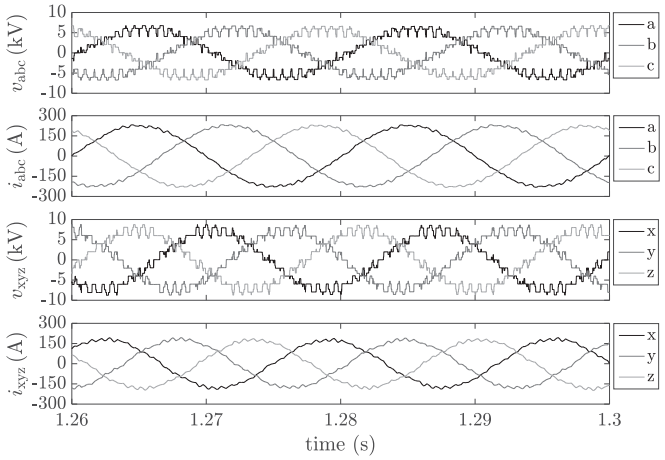

Fig. 15. Steady-state voltage and current waveforms.

the proper SMs at each time. This is done according to the sorted queue of capacitor voltages and arm current direction [22].

V. SIMULATION RESULTS

The theoretical findings for a 3-phase SMMC shown in Fig. 5 are validated by simulation using MATLAB/Simulink software. In this simulation, the HB-side of the converter is connected to Grid H with frequency of 60 Hz, while the other side is connected to Grid F operating at 50 Hz. The converter is rated for 4 MVA and the capacitors' average voltage are regulated at 2 kV. Table I lists the main simulation parameters. A multi-carrier PWM is applied to the converter such that the effective frequency of the output voltage is 1500 Hz. By having four SMs in each arm, the switching frequency of SM IGBTs is approximately 375 Hz, while the unfolder switches operate at corresponding AC line frequency. In practice, the number of levels is higher according to the desired power and AC-side voltages. Thus, the waveform quality would improve and smaller AC filters could be installed.

Fig. 15 shows the steady-state voltages and currents. The active power flows from Grid F to Grid H, while the power factor for both sides is unity. Therefore, the FB- and HB-sides of the converter operate as a rectifier and an inverter, respectively. It can be seen that the third harmonic component of the AC-side voltages is cancelled out and the desired fundamental portion is well synthesized. It must be noted that the voltages shown in Fig. 15 are considered as internal parameters of the converter and located before the AC-side filters. As mentioned in the previous section, on each side of the converter, a current controller

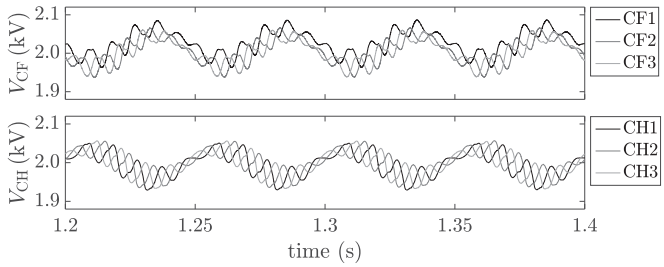

Fig. 16. Steady-state average HBA and FBA capacitor voltages.

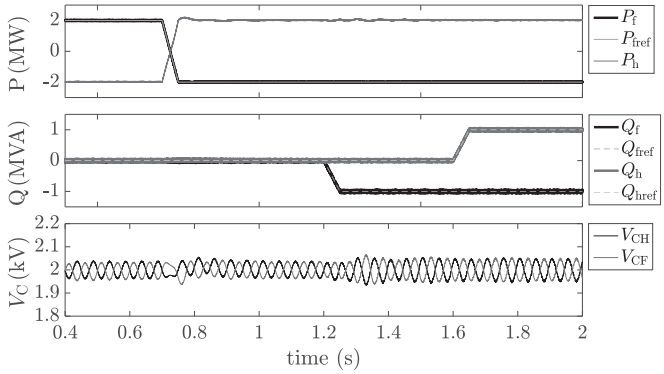

Fig. 17. Converter transient waveforms during power variation.

is utilized to ensure an AC sinusoidal current with acceptable harmonic content (see Fig. 12). The current controller is fast enough to mitigate the impact of capacitor voltage ripple on the current by modifying the converter's AC-side voltage.

Fig. 16 illustrates the behavior of the capacitor voltages in the steady-state condition. The peak-to-peak ripple in the capacitor voltage is approximately 8% which may vary due to the operating point of active and reactive powers on both sides of the converter. Since the injected third-harmonic voltage does not create current, third-harmonic frequency does not appear in capacitor voltages. The 20 Hz ripple is caused by the converter's natural energy balancing cycle. Note that the frequency of the rectified AC-voltages (and consequently current) gets doubled (i.e. 100 Hz & 120 Hz) and afterwards, the greatest common factor (GCD) of the rectified currents' frequencies appears as the natural frequency of converter's energy balancing cycle (here, $\mathrm{GCD}(100, 120) = 20$ Hz). To study the dynamic response of the converter, a few active and reactive power changes are applied on both sides as rising/falling ramp within 5 ms. As shown in Fig. 17, the desired operating point is properly controlled by its reference. During each transient, a small error may occur in the capacitor voltages which will be compensated in a few cycles.

VI. EXPERIMENTAL RESULTS

Fig. 18 shows a low-scale single-phase 5-level SMMC constructed using MOSFET devices (MTD6N15T4G). The control system is implemented on a dSPACE-MicroLabBox unit. In this setup, the HB-side of the converter is connected to the grid (120 V & 60 Hz), while the FB-side feeds a resistive load operating at 98 V & 50 Hz. The parameters of the experimental setup can be found in Table II. Here, the switching

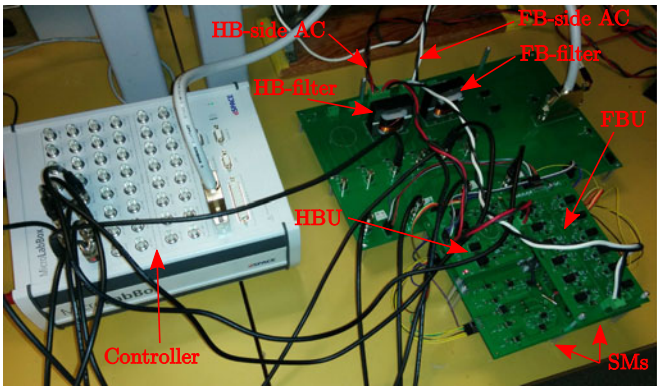

Fig. 18. A view of the experimental setup.

TABLE II
EXPERIMENTAL PARAMETERS

Parameter		Rating
HB & FB sides' frequency	$f_{\rm h}$, $f_{\rm f}$	60 Hz, 50 Hz
HB & FB sides' AC voltage (rms)	$V_{\rm ac\_h}$, $V_{\rm ac\_f}$	120 V, 98 V
SM capacitor	$C_{\rm SM}$	820 μF
Mean cell capacitor voltage	E	100 V
MOSFET maximum drain-source voltage	$V_{\rm DS}$	150 V
MOSFET continuous drain current	$I_{\rm D}$	6 A
MOSFET drain-source on-state resistance	$R_{\rm DS-ON}$	300 mΩ
Filter inductance	$L_{\rm S}$, $L_{\rm L}$	5 mH

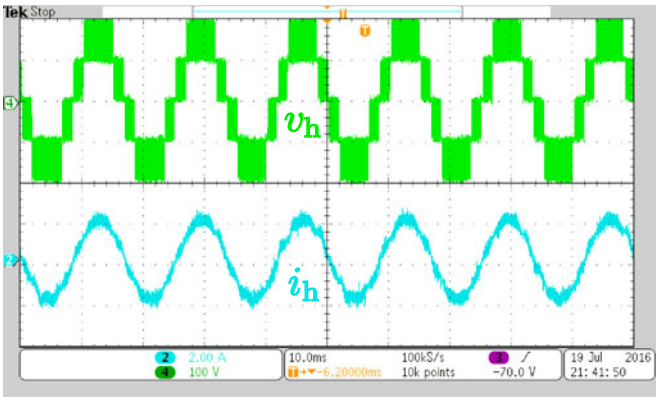

Fig. 19. Converter's HB-side waveforms in steady-state condition.

frequency of 3 kHz is applied to the SM switches which could be reduced by utilizing higher number of SMs. For a single-phase SMMC without third-harmonic injection and with frequency ratio of $60/50 = 1.2$, the voltage ratio is constant and almost equals $V_{\rm mf}/V_{\rm mh} \approx 0.81$. The reactive power on both sides are set to zero. With transferring only active power, in order to achieve power balance, the current ratio is expected to be $I_{\rm mf}/I_{\rm mh} \approx 1.23$.

The converter's HB- and FB-side steady-state waveforms are shown in Figs. 19 and 20, respectively. Both side currents are measured as they enter the converter and the voltages are measured before the AC-side filters (see Fig. 6). It can be seen that both side voltages are well synthesized with the expected amplitude and frequency.

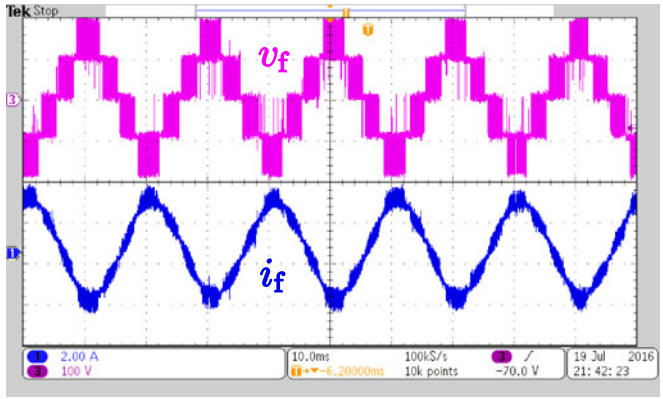

Fig. 20. Converter's FB-side waveforms in steady-state condition.

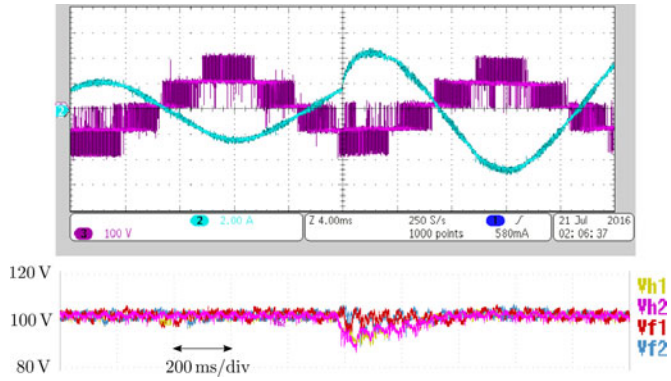

Fig. 21. Dynamic response of the converter to the load change.

In order to evaluate the dynamic response of the capacitor voltage balancing strategy, the load is suddenly doubled while the SM capacitor voltages are monitored. As shown in Fig. 21, a sudden increase in the load causes the capacitors to lose a small portion of their stored energy which would be detected by both HBA and FBA energy balancing units (see Figs. 13 and 14). Thus, the operation point will be upgraded and the capacitors' energy will be restored in less than 300 ms.

VII. CONCLUSION

The proposed control strategy ensures the capacitor voltage balancing in different operating frequencies by injecting third harmonic voltage component which is crucial to fully exploit the capabilities of a SMMC. Also, a modification of SMMC is suggested to improve the converter's performance. Both simulation and experimental results show that SMMC can fulfill the requirements of a bidirectional AC/AC converter.

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